IN THE SPECIFICATION:

Please amend the appropriate paragraphs of specification in accordance with proposed changes as outlined hereinbelow:

Please amend the paragraph on page 6, numbered lines 14 and 15, as follows:

Figs. 3a and 3b show ~~Fig. 3 shows~~ the configuration of a video processing circuit 4 shown in Fig. 1;

Please amend the last full paragraph on page 9, numbered lines 15 through 28, as follows:

Moreover, when the video input-output circuit transfers data to or from the local memory 9, the video input-output circuit issues a memory access request to the memory access controller 5 over the signal line S1. The memory access controller 5 judges the priority of the bus connector 6. If the local memory 9 is available, the memory access controller 5 transmits an access enabling signal to the video input-output circuit over the signal line S2. Furthermore, the bus connector 6 is closed in order to connect the video input-output circuit 3 to the local memory bus B2 by way of the local bus B3. At the same time, the connectors 7 and 8 are opened in order to unlink the local bus B4 and system bus B1 from the local memory bus B2.

Please amend the first full paragraph on page 10, numbered lines 1 and 2, as follows:

Figs. 3a and 3b show ~~Fig. 3 shows~~ the configuration of the video processing circuit 4 in Fig. 1.

Please amend the paragraph bridging pages 10 and 11, from numbered line 28 on page 10 to numbered line 11 on page 11, as follows:

Moreover, when the video processing circuit 4 transfers data to or from the local memory 9, the video processing circuit 4 issues a memory access request to the memory access controller 5 over the signal line S3. The memory access controller 5 judges the priority of the bus connector 7.

If the local memory 9 is available, the memory access controller 5 transfers an enabling signal over the signal line S4. Furthermore, the bus connector 7 is closed in order to link the local bus B4 and the local memory bus B2. The connectors 6 and 8 are opened in order to unlink the local bus B3 and system bus B1 from the local memory B2.

Please amend the first full paragraph on page 11, numbered lines 12 through 18, as follows:

Fig. 3b shows in detail the configuration of the motion estimation circuit/motion compensation circuit 43 shown in Fig. 3a. The bus B1 is connected to [a] an instruction register 431, a status register 432, data ~~registers~~ register 433, and memory 434[,] . The bus B4 is connected to a data ~~resister~~ register 437, memory 438 and a bus controller 436.

Please amend the paragraph bridging pages 13 and 14, from numbered line 8 on page 13 to numbered line 8 on page 14, as follows:

Fig. 6 shows a third embodiment of the signal processing circuit in accordance with the present invention. The present embodiment is adapted to a video processing integrated circuit that processes image data. The present embodiment has not only the capability of the video processing circuit, which is employed in the second embodiment, but also the capability of a circuit for processing another type of signal. A serial data input-output circuit 21 having input-output terminals P5 and P6 is included additionally. Serial data includes a compressed video signal and a compressed sound signal. Compared with an ordinary video signal, the compressed signal requires a lower transfer rate and a smaller storage capacity because it is compressed. Moreover, the compressed signal can be processed by the microprocessor 2. Therefore, the serial data input-output circuit 21 is connected to the system memory bus B1. When the serial data input-

output circuit 21 must transfer serial data, the serial data input-output circuit 21 applies an interrupt signal to the processor 2 over a signal line S9. The microprocessor 2 senses the interrupt, and controls data transfer to or from the serial data input-output circuit 21 [20]. The video data processing sequence, and the configurations and actions of the circuits are identical to those implemented in the embodiment shown in Fig. 1. The same reference numerals will be assigned to identical components, and the description of the components will be omitted.

Please amend the paragraph bridging pages 14 and 15, from numbered line 9 on page 14 to numbered line 6 on page 15, as follows:

Fig. 7 shows a fourth embodiment of the signal processing circuit in accordance with the present invention. The present embodiment is adapted to a video processing integrated circuit that processes image data. According to the present embodiment, the microprocessor 2 accesses a status register 441 and an instruction register 442, which are included in the video processing circuit 4, in response to a cyclic interrupt signal T1 produced by a timer 23. The status register 441 is a register that indicates the current state of the video processing circuit 4. The simplest information is information that processing is under way if there is any such processing, and indicated with a flag. The instruction register 442 [422] is a register that indicates an instruction which the microprocessor 2 wants the video processing circuit 4 to execute. The video processing circuit 4 executes an instruction indicated in the instruction register 442 [422]. Specifically, the video processing circuit 4 cyclically reads the status register 441 [421] in response to the interrupt signal Tl sent from the timer 23 [2]. The microprocessor 2 judges whether an instruction may be issued to the video processing circuit 4. If the video processing circuit 4 can receive the instruction, the microprocessor 2 issues an instruction to the instruction register 442 [422].

Please amend the paragraph on page 15, from numbered line 7 to numbered line 22, as follows:

Owing to the routing and the control sequence for controlling a local memory bus access authority that are features of the present invention, the performances of the microprocessor, video input-output circuit or sound input-output circuit, and video processing circuit can be utilized to the greatest possible extent. In particular, when it comes to image processing, a large amount of image data is written in or read from the local memory 9. By controlling the connection circuits 6, 7, and 8, data transfer between the local memory 9 and microprocessor 2 can be achieved in parallel with data transfer between the local memory 9 and video input-output circuit 3 or video processing circuit 4. Moreover, data can be directly transferred between the local bus B2 and system bus Bl without intervention of a register. This results in high-speed processing.